REMARKS:

This paper is herewith filed in response to the Examiner's Office Action mailed on October 10, 2007 for the above-captioned U.S. Patent Application. This office action is a rejection of claims 1-17 of the application.

More specifically, the Examiner has rejected claims 1-17 on the grounds of non-statutory obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Application No. 10/740,034; rejected claims 1-17 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; rejected claims 1 and 7 under 35 USC 102(e) as being anticipated by Karam (US7,111,089); and rejected claims 1-17 under 35 USC 103(a) as being unpatentable over Hoskins (US6,789,132) in view of Kaihlaniemi (US6,370,591). The Applicant respectfully traverses the rejections.

The Applicant notes claims 1-4, 7-10, and 12-16 have been amended for clarification. Claims 18-20 have been added. Support for the amendments and new claims can be found at least on page 4 lines 2-6, and on page 5 line 18 to page 6 line 14. No new matter is added.

Regarding the non-statutory obviousness-type double patenting rejection, the Applicant submits the attached terminal disclaimer. The double patenting rejection is seen as overcome and the rejection should be removed.

Regarding the rejections under 35 USC 112, second paragraph, as stated above claims 1, 3, 4, 7, and 13 have been amended for clarification. Further, in the rejection the Examiner states:

> "Claim 1, line 3, it is unclear what "a Dynamic Configurable Hardware Logic layer" is <i.e. how is it different from any device or hardwares that are attached to a computer?>. lines 5-6, it is unclear what a "TiEred Multimidia Acceleration Scheduler" is <i.e. how is it different from any other schedulers?>. Claims 7 and 13 have the same deficiencies as claim 1 above. ii) Claim 2, it is unclear what a "Tier-I scheduler" and a "Tier-2 scheduler" are and how they are different from each other <i.e. what are their functions? How are they distinguished from other schedulers and each

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other?>. Claims 8 and 14 have the same deficiencies as claim 2 above. iii) Claim 4, it is uncertain as to what is meant by "one context plane" <i.e. what defines a context plane?>. Claims 10 and 16 have the same deficiencies as claim 4 above."

Regarding claims 1, 7, and 13 under 35 USC 112, second paragraph, the Applicant submits that "a Dynamic Configurable Hardware Logic layer" has been clarified at least where claims 1, 7, and 13 have been amended to recite in part "a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs) dynamically configured to execute applications on the device." In addition, these claims have been further amended for clarification to include that the TEMAS cooperates with the OS scheduler for scheduling and for prioritizing the applications. The Applicant contends that in claims 1, 7, and 13 a clear distinction for "a Dynamic Configurable Hardware Logic layer" and the "TiEred Multi-media Acceleration Scheduler (TEMAS)" is evident, thus the rejections of claims 1, 7, and 13 under 35 USC 112, second paragraph, of these claims are seen as overcome.

Regarding the rejection of claims 2, 8, and 14 under 35 USC 112, second paragraph, the Applicant notes that the claims have been amended in a similar manner to recite in part "where the at least one Tier-2 scheduler communicates with the Tier-1 scheduler and the DCHL, allowing different DCHL to be compatible with a generic OS scheduler." The Applicant contends that for at least this reason the Tier-1 scheduler and a Tier-2 scheduler are seen as distinguished from "other schedulers and each other" as indicated by the Examiner. Thus, the rejections under 35 USC 112, second paragraph, of claims 2, 8, and 14 under 35 USC 112, second paragraph, are seen as overcome.

Regarding the rejection of claims 4, 10, and 16 under 35 USC 112, second paragraph, the Applicant notes that claim 4 has been amended for mere clarification to recite "A device architecture as in claim 1, where said plurality of LEs are in at least one context arranged in at least one context plane." Further, claims 10 and 16 have been similarly amended. The Applicant submits that the term "context" is understandable to an ordinary person skilled in the art, thus the term context plane can be seen to relate to an arrangement of the contexts of the LEs. The Applicant contends that the rejections under 35 USC 112, second paragraph, of claims 4, 10, and 16 are seen as overcome.

For at least the reasons stated the rejection of claims 1-17 under 35 USC 112, second paragraph, are now seen as overcome and the Applicant respectfully requests that the Examiner remove the rejections.

Regarding the rejections of claims 1 and 7 under 35 USC 102(e) over Karam the Applicant notes that the attached Declaration under Rule 131 disqualifies Karam as prior art against this application. More specifically, Exhibit A as referenced by the declaration shows conception at least as early as December 13, 2002. The earliest date for Karam is seen to be December 23, 2002.

The undersigned attests to the following as to diligence. The docket/reference numbers NC39080 and 883.0005.U1(US) each refer to the subject matter of this application. Exhibit A is an invention report based thereon that was considered by a patent committee of the Nokia Corporation of Espoo, Finland, December 13, 2002 as evidenced by the date stamp in the footnote area of the filename.ppt pages 1-4 of Exhibit A. This independently proves the asserted date of conception. Further, on December 13, 2002 the Nokia Corporation tasked the firm Harrington & Smith LLP to prepare and file a non-provisional US patent application based on that subject matter, as evidenced by Exhibit B. It is further noted that the entirety of Exhibit A was attached to the Exhibit B when Exhibit B was sent to the firm Harrington & Smith LLP.

It is noted that in Exhibit A information has been redacted from page 1 and pages 2-4. Further, information has been redacted from Exhibit B. The Applicant submits that the information that was excluded from Exhibits A and B, as indicated above, is not relevant to the Declaration, conception, or diligence.

A Provisional US patent application was filed on December, 26, 2002, of which the present application claims priority.

The undersigned attests that exhibits A and B are true copies; acknowledges that statements made above are true or made on information believed to be true; and further acknowledges that any willful false statements are punishable by fine or imprisonment or both under 18 USC 1001.

Therefore, for at least the reasons stated conception is shown prior to the earliest date of Karam and diligence is shown from then until constructive reduction to practice which occurred no later than December 26, 2002 when the priority application to the one now pending was filed with the US patent office. Karam is not prior art against this application.

Regarding the rejection of claims 1-17 under 35 USC 103(a) the Applicant notes that claim 1 has been amended for clarification to recite:

> A device architecture for running applications, comprising: an operating system (OS) comprising an OS scheduler; a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs) <u>dynamically configured to execute applications on the device</u>; interposed between said OS and said DCHL layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) that cooperates with the OS scheduler for scheduling <u>and for prioritizing the applications;</u> and <u>based on the scheduling and the priority,</u> configuring <u>at least some of</u> the <u>plurality of</u> LEs of the DCHL to execute <u>the</u> applications.

In the rejection of claim 1 the Examiner states:

> "As per claims 1 and 7, Hoskins teaches a device architecture for running applications, comprising: **a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs) (Fig 2, unit 110 and all of unit 202 except unit 222)**; and interposed between a host computer (Fig 2, unit 200) and said DCHL layer, **a TiEred Multi-media Acceleration Scheduler (TEMAS) (Fig 2, unit 222) that cooperates with the host computer for scheduling and configuring the LEs of the DCHL to execute applications (Column 5, lines 35-39; Column 6, lines 1-10, lines 41-47).** 12," (emphasis added).

Firstly, regarding Figure 2 the Applicant notes that immediately preceding the citation by the Examiner, Hoskins discloses:

> "Referring now to FIG. 2, shown therein is a functional block diagram of the disc drive 100 of FIG. 1, **generally showing the main functional modules which control the operation of the disc drive 100,**" (emphasis added), (col. 5, lines 31-35).

The Applicant notes that the Examiner apparently has equated the plurality of Logic Elements of claim 1 with "unit 110 and all of unit 202 except unit 222" of Hoskins. The

Applicant respectfully submits that Hoskins discloses that these units are "functional modules" and that **these functional modules relate to the operation of the disk drive 100**. Further, Hoskins discloses "Information is written to and read from tracks on the discs 108 through the use of an actuator assembly 110," (col. 4, lines 55-56). Clearly, neither the functional modules nor the actuator assembly 110 in Hoskins, as cited by the Examiner, can be seen to relate to a Dynamic Configurable Hardware Logic layer comprised of **Logic Elements that are dynamically configured to execute applications**. As stated above, these features of Hoskins are merely seen to relate to the operation of the disk drive 100. The Applicant submits that Hoskins does not appear to disclose or suggest that the Logic Elements and the actuator assembly of Hoskins are executing applications on the device. Rather, the Applicant submits that the operation of the functional modules is seen to generate instructions for use by the actuator arm on the disc 108 in order to read and write data on the disc. The Applicant contends that the references cited at least can not be seen to disclose or suggest "a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs) **dynamically configured to execute applications on the device**," as in claim 1.

Furthermore, in regards to unit 222 of Figure 2, the Applicant respectfully notes that in several locations Hoskins indicates that the operational flow of the scheduler module 222 is performed in a circular manner, (col. 13, lines 22-24; col. 14, lines 40-41; col. 18, lines 32-32). The Applicant contends that the scheduler module 222 in Hoskins does not relate a TiEred Multi-media Acceleration Scheduler (TEMAS) for **scheduling and for prioritizing** of applications as in claim 1. The Applicant notes that the scheduler module 222 merely relates to a scheduler that maintains **a circular operational flow** in order to dispatch the functional modules to operate the disk drive 100 of Hoskins.

Further, Hoskins discloses:

> "In a preferred embodiment of the present invention the host module 224, the queue processor module 228, the active command module 232, and the disc/servo module 236 are all cooperative and cannot be preempted by another module scheduled by the scheduler 222. **As such, no modules scheduled by the scheduler 222 require context saves when being implemented by the scheduler 222, thus reducing the switching time between one module and another and allowing quicker response time**

to time critical events then would occur if the modules were preemptive," (emphasis added), (col. 7, lines 30-39).

The Applicant submits that here Hoskins appears to indicate that no module is preemptive of another module. Thus, it appears that the scheduler module 222 in Hoskins at least does not relate to a priority of applications as in claim 1.

Clearly, for at least the reasons stated the scheduler module 222 can not be seen to relate to a TiEred Multi-media Acceleration Scheduler (TEMAS) for **scheduling and for prioritizing** of applications as in claim 1.

For at least the reasons stated the Applicant contends that the references cited can not be seen to disclose or suggest claim 1.

In addition, for at least the reason that claims 7 and 13 recite features similar to claim 1 as stated above, the references cited can not be seen to disclose or suggest all claims 1, 7, and 13.

In regards to the rejection of claims 2, 8, and 14 under 35 USC 103(a) the Examiner states:

> "As per claims 2, 8,14, Hoskins teaches where the TEMAS is comprised of a Tier-1 scheduler that communicates with the OS scheduler and at least one Tier-2 scheduler (Fig 3, units 303, 305, and 307) interposed between the Tier-1 scheduler and one DCHL configurable device (Column 6, lines 50-57; Column 8, lines 39-44)."

Claim 2 recites:

> A device architecture as in claim 1, where the TEMAS is comprised of a Tier-1 scheduler that communicates with the OS scheduler and at least one Tier-2 scheduler interposed between the Tier-1 scheduler and one DCHL configurable device, where the at least one Tier-2 scheduler communicates with the Tier-1 scheduler and the DCHL, allowing different DCHL to be compatible with a generic OS scheduler

As cited by the Examiner Hoskins discloses:

> **"the scheduler module 222 includes four module launch points 301, 303, 305, and 307, each of which corresponds to an associated module:** the host module 224, the queue processor module 228, the active command

module 232, and the disc/servo module 236, respectively," (emphasis added), (col. 6, lines 54-57).

Firstly, the Applicant contends that Hoskins does not disclose or suggest a Tier-1 scheduler that communicates with the OS scheduler as in claim 2. Further, Applicant can find nothing in Hoskins to disclose or suggest that a Tier-2 scheduler communicates with a Tier-1 scheduler and the DCHL allowing different DCHL to be compatible with a generic OS scheduler as in claim 2. For at least these reasons the references cited are not seen to disclose or suggest claim 2. Thus, the rejection of claim 2 should be removed.
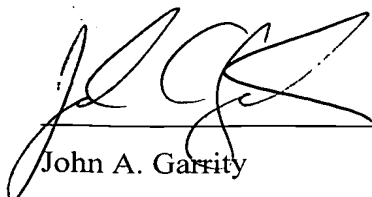
In addition, for at least the reason that claims 8 and 14 recite similar features of claim 2 as stated above, the references cited are not seen to disclose or suggest all claims 2, 8, and 14.

Further for at least the reason that claims 2-6 and 18; claims 8-12 and 19; and claims 14-17 and 20 depend from claims 1, 7, and 13, respectively, the references cited can not be seen to disclose or suggest all claims 1-20.

Based on the above explanations and arguments, it is clear that the references cited cannot be seen to disclose or suggest claims 1-20. The Examiner is respectfully requested to reconsider and remove the rejections of claims 1-20 and to allow all of the pending claims 1-20 as now presented for examination.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted:

John A. Garrity

2/11/2008

Date

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